Ausdia Introduces Hierarchical Budget Analysis and Asynchronous Glitch Detection Add-ons to Timevision at DAC 2015

Add-ons generate, verify and refine hierarchical timing budgets; screen and locate "glitchy" logic; and reduce analysis noise

Mountain View, California – June 4, 2015– Ausdia, the leading developer of timing constraints verification and management solutions that complement timing signoff for complex system-on-chip (SoC) designs, will introduce two add-on options to its comprehensive Timevision™ solution at DAC 2015. Timevision Hierarchy Budgets generates hierarchical timing budgets from design logic, verifies that design engineers are not over- or under-constraining designs, and automatically fixes any issues by re-budgeting. Timevision Glitch Detection is a formal-analysis-based check and root-cause locator that easily and quickly locates glitches due to false paths, reconvergence, and clock/ data reconvergence on asynchronous crossings.

SoC designs at 16nm and 10nm are getting larger and more complicated as more and more functionality is placed into designs, requiring virtually all designs to be implemented hierarchically. In addition, the increased number of clock domains and the prevalence of gating structures to reduce power are making it more likely, statistically, that "glitches" (momentary but short-lived logic changes) are going to be created, sampled, and make it into the design itself. Glitches are often silicon killers, and it can take months of painstaking analysis in a lab setting to pinpoint the problem.

Timevision is a comprehensive timing constraints development, verification and management solution that complements all implementation and timing signoff flows, with the capacity to handle over one billion cells and 1000s of clocks. Introduced at DAC 2012, Timevision integrates with all aspects of the design flow and is used before synthesis, before DFT insertion, before place and route, and when signoff timing is being run. Timevision helps designers create good SDC/TCL constraints and is a verification platform for existing timing constraints.

Timevision Hierarchy Budgets

Budgets are sometimes created manually and sometimes automatically. In all cases, though, design engineers struggle to understand if they are correct and to ensure that

silicon is not over- or under-constrained, which results in poor or untuned quality of results. Timevision Hierarchy Budgets leverages Ausdia's leading "unlimited capacity" solution for timing and hierarchical analysis to help designers converge on timing closure faster and more accurately, without excessive optimization that wastes power and area.

Timevision Glitch Detection

When designs are transformed from RTL description to gates, the synthesis and layout tools can do a lot of Boolean optimization on the circuits. However, in the case of certain asynchronous logic crossings, the tools can do something that is logically correct but that creates a logic glitch in silicon. Timevision Glitch Detection is a formal-analysis-based check and glitch locator that easily and quickly screens and locates glitches due to false paths, reconvergence and clock/data reconvergence on asynchronous crossings. It uses a novel combination of Ausdia's timing engine, high-performance structural analysis, and formal verification to complete a low-noise, high-speed analysis and ensure that the actual silicon does not have any glitchy logic.

"Our customers are completing their SoC designs using hierarchical design flows and verifying that their silicon is going to be first-time successful when they release to the factory," said Ausdia president and CEO Sam Appleton. "We're introducing Glitch Detection to allow our formal analysis engine to be applied to a true "silicon signoff" problem that is very important before release to factory, and to eliminate a potential source of reliability and yield issues in real silicon. Hierarchical SoC implementation continues to be difficult to execute, and our Hierarchical Budgets feature is the first in a range of features to help alleviate this problem."

Pricing and Availability

Timevision Hierarchy Budgets and Timevision Glitch Detection are available now. Pricing for a one-year worldwide time-based license (TBL) is $7,500 for each add-on option.

Ausdia is exhibiting Timevision and all add-ons in Booth # 826 at the 52nd Design Automation Conference (DAC) in San Francisco, from June 8th through 10th, 2015.

About Ausdia

Ausdia delivers standout timing constraint development, verification, and management solutions that complement all implementation and timing signoff flows. The company's groundbreaking methodology and products give system-on-chip (SoC) and integrated circuit (IC) developers a new way to work, enabling massive productivity gains throughout the design flow. Founded in 2006, the privately-held company is headquartered in Sunnyvale, California.

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